**Amendments to the Claims:**

The listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1 – 2 (cancelled)

Claim 3. (currently amended) A programmable controller for use with a monitoring device, said programmable controller including:

at least one digital input interface,

at least one digital output interface for receiving data from at least one output register,

programmable logic hardware including a plurality of ~~basic~~ logic elements including flip-flops, and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a logic circuit, said logic processing circuit arranged to implement a user control program defined by a user as a user control program circuit, said logic processing circuit configurable in said programmable logic hardware, and connected to said input interfaces and said output interfaces,

program loading circuits for configuring said ~~to enable the user to configure the~~ programmable logic hardware with said logic processing ~~a circuit including said user program~~ circuit prior to initiating control, and where ~~wherein:~~said programmable logic hardware, ~~is~~ configured with the logic processing circuit, includes:

a plurality of logic processing circuit flip-flops for storing state data, and for each of these flip-flops, an associated support circuit, the support circuits arranged to operate selectively between first and second conditions, wherein in said first condition the support circuits connect the flip-flops as a shift register for transporting state data into and out of the logic processing circuit, and wherein in the second condition the support circuits connect the flip-flops as logic elements of said user control program, the support circuits being selected to operate in only one of either the first condition or the second condition at any one time~~including at least two functionally separate subsystems, a first subsystem comprising~~

~~said user program circuit, and a second subsystem to provide monitoring services and to control the operation of said user program circuit, wherein:~~

~~said first subsystem has a plurality of flip-flops combined with gating circuits, wherein one of said flip-flops combined with one of said gating circuits forms a dual purpose flip-flop for storing state data in said user program circuit, said dual purpose flip-flops, when connected in said user program circuit, are selectively operable in a first way as a shift chain operable to provide both read and write access to said state data or in a second way as logic elements of said user program circuit, only one of said first way or said second way being operative at any one time~~.

Claim 4. (currently amended) The programmable controller as claimed in claim 3, further including:

a monitoring services and control unit arranged to control and operate said logic processing circuit in at least two individually selectable modes of operation, and said logic processing circuit arranged to operate in a continuously repeating logic processing circuit scan cycle, and

whereby in a first mode, said monitoring services and control unit is arranged to operate said support circuits in said first condition, to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops, but not in said second condition,

whereby in a second mode, said monitoring services and control unit is arranged to operate said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged to operate to shift state data out of and into said logic processing circuit to provide read and write access to said first plurality of logic processing flip-flops; and when in said second condition said programmable controller is arranged to operate to sample and store the value of at least one input signal from said at least one digital input interface, to apply user clock pulses to said logic processing circuit and to update said at least one output register~~wherein,~~

~~said second subsystem enables the control and operation of said user program circuit in a plurality of modes of operation in response to commands from the monitoring computer, said modes of operation including:~~

~~a logic processing mode in which said dual purpose flip-flops are operated as~~

~~said logic elements in said user program circuit, and in which the clock to said dual purpose flip-flops is enabled, or~~

~~a pause mode in which the clock to said dual purpose flip-flops is disabled, and wherein either said logic processing mode or said pause mode may be temporarily interrupted by a data access mode in which said dual purpose flip-flops are operated as part of a shift chain so that enabling the clock to said dual purpose flip-flops shifts the state data in said dual purpose flip-flops and provides both read and write access.~~

Claims 5 – 7 (cancelled)

Claim 8. (previously presented) The programmable controller as claimed in claim 4 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register, and

state data relocation means for writing, within one data access interval, state data from an outgoing said programmable logic hardware section to the state data storage units of an incoming said programmable logic hardware section that have the same user control program functions as those from which it was read.

Claim 9. (previously presented) The programmable controller as claimed in claim 8, wherein said state data relocation means comprises:

relocation address storage writable by said monitoring device, corresponding with said state data storage units,

secondary state data storage to save data from said state data storage units,

selection means for selecting either a non-relocated address or a relocated address with which to access said secondary state data storage, and

data relocation means for performing, within one said data access interval, the steps of:

(i) reading a state data bit from said outgoing programmable logic hardware section,

(ii) writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,

(iii) repeating steps (i) and (ii) until all required bits have been relocated and transferred,

(iv) reading a state data bit from said secondary state data storage,

(v) writing said state data bit into said incoming programmable logic hardware section at the same address at which it was located in said secondary state data storage, and

(vi ) repeating steps (iv) and (v) until all required bits have been transferred.

Claim 10. (previously presented) A programmable controller said programmable controller including:

at least one input interface and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,

at least one output interface for connection to process plant and/or machinery to receive output data in digital form,

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a user control program circuit and to connect the user control program circuit to said input and output interfaces,

program loading means to enable the user to configure the programmable logic hardware as a circuit implementing a user control program prior to initiating control of the associated process plant and/or machinery,

a user control program implemented as an electrical logic circuit configured in said programmable logic hardware, with said user program circuit connected to said input and output interfaces and means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and

indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

Claim 11. (previously presented) A programmable controller said programmable controller including:

at least one input interface and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,

at least one output interface for connection to process plant and/or machinery to receive output data in digital form,

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a user control program circuit and to connect the user control program circuit to said input and output interfaces,

program loading means to enable the user to configure the programmable logic hardware as a circuit implementing a user control program prior to initiating control of the associated process plant and/or machinery,

a user control program implemented as an electrical logic circuit configured in said programmable logic hardware, with said user program circuit connected to said input and output interfaces and

means to support circuit failure detection and connection including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and

failure detection means to compare a set of output values of each said programmable logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs via the output register and ensure incorrect output values as indicated by said failure detection means do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic

hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that programmable logic hardware section.

Claim 12. (previously presented) The programmable controller as claimed in claim 10 including a plurality of said failure detection means with the sets of outputs from each section of programmable logic hardware provided as inputs to each said failure detection means, and

detection of a failure by any one of the two or more failure detection means indicates that a failure has occurred.

Claim 13. (previously presented) The programmable controller as claimed in claim 11 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

Claim 14. (previously presented) The programmable controller as claimed in claim 13 including exception evaluating and handling means which ensures that the controller responds appropriately when the number of sets of concurrently correct output values deemed desirable as a safety margin does not exist, the minimum said number being two.

Claim 15. (previously presented) The programmable controller as claimed in claim 3

wherein said programmable controller receives input signals from duplicate sensors and said user control program includes at least one input signal monitoring function block, said monitoring block determining the invalidity of an input signal by a comparison of said duplicate input signals using criteria defined as part of the function block as suitable to identify signals in error, and indicating an input signal error if said input signal is deemed invalid.

Claim 16. (previously presented) The programmable controller as claimed in claim 15 wherein said duplicate sensors include three or more matching sensors and the respective said input signal monitoring function block determines the invalidity of an input signal from a comparison of said matching input signals, and determines the invalid signal as the odd-one-out, and passes a single copy of the valid signals as the input signal.

Claim 17. (previously presented) The programmable controller as claimed in claim 4 including means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

Claim 18. (previously presented) The programmable controller as claimed in claim 4 including means to support circuit failure detection and correction including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and

said identical input valves provided in a way so as to be settled and not transient at the time of sampling by the user control program circuit, and

failure detection means to compare a set of output values of each said programmable

logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs via the output register and ensure incorrect output values as indicated by said failure detection means do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that programmable logic hardware section.

Claim 19. (previously presented) The programmable controller as claimed in claim 18 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

Claims 20 – 21(cancelled)

Claim 22. (currently amended) The programmable controller as claimed in claim 4, wherein said monitoring services and control unit is arranged to:

operate said at least one output register, when said support circuits are operated according to said first condition, to maintain the level of the output signal(s) to said at

least one digital output interface at defined levels, said levels being defined by the levels last sampled from the user control program circuit when said support circuits were operated according to said second condition:

~~said programmable controller may be set to operate said user program circuit in said logic processing mode, and when so set is able to respond to the monitoring computer to enable access to the state data in said user program circuit and in so doing said user program circuit enters said data access mode, and during such an instance of said data access mode entered from a said logic processing mode, said output registers maintain the system output signals at the levels last established by said logic processing mode, but when data access is complete, said user program circuit is automatically switched back to said logic processing mode and said user program circuit again updates said output registers, and~~

~~said programmable controller may be set to operate said user program circuit in said pause mode, and when so set is able to respond to the monitoring computer to enable access to said user program circuit state data and in so doing said user program circuit enters said data access mode, but when data access is complete, said user program circuit is automatically switched back to said pause mode~~.

Claim 23. (previously presented) The programmable controller as claimed in claim 22 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register, and

state data relocation means for writing, within one data access interval, state data from an outgoing said programmable logic hardware section to the state data storage units of an incoming programmable logic hardware section that have the same user control program functions as those from which it was read.

Claim 24. (previously presented) The programmable controller as claimed in claim 23, wherein said state data relocation means comprises:

relocation address storage writable by said monitoring device, corresponding with said state data storage units,

secondary state data storage to save data from said state data storage units,

selection means for selecting either a non-relocated address or a relocated address with which to access the said secondary state data storage, and

data relocation means for performing, within one said data access interval, the steps of:

(i) reading a state data bit from a programmable logic hardware section,

(ii) writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,

(iii) repeating steps (i) and (ii) until all required bits have been relocated and transferred,

(iv) reading a state data bit from said secondary state data storage,

(v) writing said state data bit into the same or a different programmable logic hardware section at the same address at which it was located in said secondary state data storage, and

(vi) repeating steps (iv) and (v) until all required bits have been transferred.

Claim 25. (previously presented) The programmable controller as claimed in claim 22 including means to support state data modification comprising:

secondary modification data storage corresponding to said state data storage units, and

a modification indicator corresponding to each said state data storage unit, said modification indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means operative to perform within one said data access interval the steps of:

scanning said modification indicators,

loading data stored in said secondary modification data storage units to said corresponding state data storage units if the corresponding modification indicator so indicates, and

resetting said modification indicators.

Claim 26. (previously presented) The programmable controller as claimed in claim 22 including means to support state data forcing comprising:

secondary modification data storage corresponding with said state data storage units;

a data forcing indicator for each said storage unit, said data forcing indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means for performing within one said data access interval the steps of:

scanning said data forcing indicators,

loading data stored in said secondary storage units to said corresponding state data storage units if the corresponding data forcing indicator so indicates,

without resetting said data forcing indicators.

Claims 27 – 28 (cancelled)

Claim 29. (previously presented) The programmable controller as claimed in claim 4 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register,

an outgoing user control program in a said section of the programmable logic hardware and,

a new user control program in another said programmable logic hardware section not connected to said output interface.

Claim 30. (previously presented) The programmable controller as claimed in claim 29 including:

state data from the outgoing said programmable logic hardware section written to the state data storage units of said programmable hardware section holding said new user control program that have the same user control program functions as those from which it was read.

Claim 31. (previously presented) The programmable controller as claimed in claim 22 arranged to enable program swapping within a single section of programmable logic hardware, including:

an outgoing logic circuit, with which items qualified by the term "outgoing" are associated, and including an outgoing user program circuit operating in said logic processing mode, and

an incoming logic circuit, with which items qualified by the term "incoming" are associated, being currently inoperative, and

performing in order the steps of:

switching the mode of said outgoing user program circuit to pause mode and preserving the value stored in said output registers,

reading the state data from said outgoing user program circuit,

configuring into said single section of programmable logic hardware an incoming logic circuit including an incoming user program circuit, said incoming user program circuit being a modification of said outgoing user program circuit,

writing the state data from said outgoing user program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a functional equivalent in said outgoing user program circuit has its state set to the same state that existed in the functionally equivalent bit in said outgoing user program circuit, and in the process relocating state data bits into different physical locations in said single section of programmable logic hardware as compared to the physical locations in said single section of programmable logic hardware from which they were read, and

switching the mode of said incoming user program circuit to said logic processing mode and enabling said output registers to be updated, wherein

a functionally equivalent bit is a bit in one of the user program circuits, either said incoming user program circuit, or said outgoing user program circuit, that has identical meaning and function as that of a bit in the other user program circuit, to which it is therefore functionally equivalent, such functionally equivalent bits always existing in pairs.

Claim 32. (cancelled)

Claim 33. (new) The programmable controller as claimed in claim 3 wherein the flip-flops connected as a shift register have their order in the shift register determined by programmable logic device configuration.

Claim 34. (new) The programmable controller as claimed in claim 4 wherein said monitoring services and control unit is further arranged to perform a program swap operation, including circuits arranged to:

configure into an incoming section of programmable logic hardware an incoming logic processing circuit including an incoming user control program circuit,

terminate the continuously repeating logic processing circuit scan of an outgoing logic processing circuit and maintain the value stored in said output registers,

maintain the output signal(s) to said at least one digital output interface at the level last sampled from the user control program circuit,

read the state data from said outgoing user control program circuit,

write the state data from said outgoing user control program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a corresponding bit in said outgoing user control program circuit has its state set to the same state that existed in the corresponding bit in said outgoing user control program circuit, said write the state data including relocating, as necessary, state data bits at different addresses in said incoming section as compared to the addresses in said outgoing section from which they were read, and

start the continuously repeating logic processing circuit scan of said incoming logic processing circuit, and enabling said output registers to be updated.

Claim 35. (new) The programmable controller as claimed in claim 33, further including a monitoring services and control unit arranged to control and operate said logic processing circuit in at least two individually selectable modes of operation, and said logic processing circuit arranged to operate in a continuously repeating logic processing circuit scan cycle, and

whereby in a first mode, said monitoring services and control unit is arranged to operate said support circuits in said first condition, to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops, but not in said second condition,

whereby in a second mode, said monitoring services and control unit is arranged to operate said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged to operate to shift state data out of and into said logic processing circuit to provide read and write access to said first plurality of logic processing flip-flops; and when in said second condition said programmable controller is arranged to operate to sample and store the value of at least one input signal from said at least one digital input interface, to apply user clock pulses to said logic processing circuit and to update said at least one output register.

Claim 36. (new) The programmable controller as claimed in claim 35, wherein said monitoring services and control unit is arranged to:

operate said at least one output register, when said support circuits are operated according to said first condition, to maintain the level of the output signal(s) to said at least one digital output interface at defined levels, said levels being defined by the levels last sampled from the user control program circuit when said support circuits were operated according to said second condition.

Claim 37. (new) The programmable controller as claimed in claim 35 wherein said monitoring services and control unit is further arranged to perform a program swap operation, including circuits arranged to:

configure into an incoming section of programmable logic hardware an incoming logic processing circuit including an incoming user control program circuit,

terminate the continuously repeating logic processing circuit scan of an outgoing logic processing circuit and maintain the value stored in said output registers,

maintain the output signal(s) to said at least one digital output interface at the level last sampled from the user control program circuit,

read the state data from said outgoing user control program circuit,

write the state data from said outgoing user control program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a corresponding bit in said outgoing user control program circuit has its state set to the same state that existed in the corresponding bit in said outgoing user control program circuit, said write the state data including relocating, as necessary, state data bits at different addresses in said incoming section as compared to the addresses in said outgoing section from which they were read, and

start the continuously repeating logic processing circuit scan of said incoming logic processing circuit, and enabling said output registers to be updated.

Claim 38. (new) The programmable controller as claimed in claim 37 further including circuits arranged to facilitate relocation of user control program circuit state data from a logic processing circuit in said outgoing section into the user control program circuit in a logic processing circuit in said incoming section, said circuits arranged to facilitate including:

relocation address memory circuits arranged to provide the address of a first bit in a pair of corresponding bits as a function of the address of the second bit in the same pair of corresponding bits.

Claim 39. (new) The programmable controller as claimed in claim 38, wherein said monitoring services and control unit is arranged to operate to perform a program swap, said programmable logic hardware arranged in separately configurable sections, said sections including:

an outgoing section, said outgoing section having an outgoing logic processing circuit arranged to operate, prior to the program swap, in a continuously repeating logic processing circuit scan cycle, and

an incoming section, said incoming section being inoperative prior to the program swap.

Claim 40. (new) The programmable controller as claimed in claim 34 further including circuits arranged to facilitate relocation of user control program circuit state data from a logic processing circuit in said outgoing section into the user control program

circuit in a logic processing circuit in said incoming section, said circuits arranged to facilitate including:

relocation address memory circuits arranged to provide the address of a first bit in a pair of corresponding bits as a function of the address of the second bit in the same pair of corresponding bits.

Claim 41. (new) The programmable controller as claimed in claim 40, wherein said monitoring services and control unit is arranged to operate to perform a program swap, said programmable logic hardware arranged in separately configurable sections, said sections including:

an outgoing section, said outgoing section having an outgoing logic processing circuit arranged to operate, prior to the program swap, in a continuously repeating logic processing circuit scan cycle, and

an incoming section, said incoming section being inoperative prior to the program swap.

Claim 42. (new) The programmable controller as claimed in claim 41 further arranged to allow the continuance of circuit operation after the occurrence of a circuit operational failure of a type that does not cause permanent physical damage to said programmable controller, including:

at least three separately configurable blocks of programmable logic hardware, each said block being equivalent to one said outgoing section and one said incoming section, and performing in order the steps of:

operating each said block in parallel and in synchronism,

identifying circuit failures, by comparing on a clock-by-clock basis the operation of each said block against each other said block, and determining when at least one said block operates differently to the other said blocks,

reconfiguring each said block that has failed and placing the non-failing said blocks in said pause mode thus preserving the value stored in said output registers,

transferring the state of the non-failing said blocks to the reconfigured said block(s), and

restarting said blocks in said logic processing mode in parallel and in synchronism and enabling said output registers to be updated.